Amendments to the Specification:

Please amend the paragraph at page 27, line 24 to page 28, line 20 as follows:

Also, in the selective gate region, the electrical connection between the wiring 21 for supplying signals to the first electrode layer 13 and the first electrode layer 13 is achieved via the second electrode layer 18 extended over the element isolating region 15. In other words, it is unnecessary to draw the first electrode layer 13 having a high ~~resistively~~ resistivity onto the element isolating region 15, making it possible to avoid the problem of the delay caused by the resistance of the first electrode layer 13 and to avoid the problem of the RC delay caused by the capacitive coupling between the semiconductor layer 11 and the first electrode layer 13. In addition, since the second electrode layer 18 is formed of a metal layer having a high melting point or a low resistance layer including a metal silicide layer having a high melting point, it is possible to avoid the problem of the resistance delay, making it possible to obtain an operating speed substantially equal to that of the transistor formed of a gate electrode layer of a single layer structure having a low resistivity. It follows that it is possible to avoid the problem that the reading speed of the memory cell is adversely affected by the increase in the delay time.

Please amend the paragraph at page 28, line 21 to page 29, line 15 as follows:

Concerning the gate of the selective gate region, the open portion ~~18~~ 17 is formed in the center of the second electrode layer 18. Therefore, the gate is of a two-layer structure consisting of the first electrode layer 13 and the second electrode layer 18. However, the gate is of a three-layer structure, consisting of the first electrode layer 13, the second electrode layer 18, and the second insulating film 16 interposed between the first electrode layer 13 and the second electrode layer 18 in the edge portion of the second electrode layer 18 in which the gate is formed. It follows that, concerning the region in which the gate is formed, the

memory cell array region and the selective gate region are equal to each other in the laminate structure of the gate. As a result, it is possible to form simultaneously the gates in the memory cell array region and the selective gate region. In addition, since a special structure is not required between the selective gate region and the memory cell array region, it is possible to set the distance D between the memory cell and the selective transistor at, for example, the minimum processing size.

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[Please amend the paragraph at page 29, lines 16-27, as follows:]

Also, in the open portion 17 of the insulating film 16, the length of the open portion 17 in a direction perpendicular to the direction of the gate length L is large, though the width of the open portion 17 in the direction of the gate length L is small. As a result, the resolution is facilitated in the lithography process in patterning the open portion ~~10~~ 17. It follows that it is possible to form a fine open portion 17 even in the case where the gate length L of the selective transistor is rendered long in accordance with miniaturization of the selective transistor.